

REMARKS

The Office Action of October 7, 2008 was received and carefully reviewed. Claims 1-14 were pending prior to the instant amendment. By this amendment, claims 1-4, 7, and 13-14 are amended. Consequently, claims 1-14 are currently pending in the instant application. Reconsideration and withdrawal of the currently pending rejections are requested for the reasons advanced in detail below.

Claims 1-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yudasaka et al. (U.S. Patent Publication No. 2002/0179906, hereinafter Yudasaka) in view of Bojkov et al. (U.S. Patent No. 5,947,783, hereinafter Bojkov). Yudasaka in view of Bojkov, however, fails to render the claimed invention unpatentable. Each of the claims recite a specific combination of features that distinguishes the invention from the prior art in different ways. For example, independent claim 1 recites a combination that includes, among other things:

“ . . . a gate electrode formed over one of the substrates by fusing conductive nanoparticles . . . a first layer including at least one of silicon nitride and nitride oxide silicon formed on and in direct contact with the gate electrode . . . a gate insulating layer at least containing a second layer comprising silicon oxide over the first layer . . . a semiconductor layer over the gate insulating layer.”

Independent claim 2 recites yet another combination that includes, *inter alia*,

“ . . . a gate electrode formed over one of the substrates by fusing conductive nanoparticles . . . a first layer including at least one of silicon nitride and silicon oxynitride formed on and in direct contact with the gate electrode . . . a gate insulating layer at least containing a silicon oxide layer over the first layer . . . a semiconductor layer over the gate insulating layer . . . a wiring connected to at least one of a source and a drain . . . a second layer including at least one of silicon nitride and nitride oxide silicon formed to be on and in direct contact with the wiring . . . wherein the wiring formed by fusing conductive nanoparticles.”

Independent claim **3** recites a further combination that includes, for instance,

“ . . . the gate electrode formed over one of the substrates by fusing conductive nanoparticles . . . a first layer including at least one of silicon nitride and nitride oxide silicon formed on and in direct contact with the gate electrode . . . a gate insulating layer at least containing a second layer comprising silicon oxide over the first layer . . . a semiconductor layer over the gate insulating layer.”

Independent claim **4** recites another combination that includes, for instance,

“ . . . a pixel electrode connected to the first thin film transistor . . . a first wiring extending from the driver circuit and connected to a gate electrode of the first thin film transistor, wherein the first thin film transistor comprises:

the gate electrode formed over one of the substrates by fusing conductive nanoparticles . . . a first layer including at least one of silicon nitride and nitride oxide silicon formed on and in direct contact with the gate electrode . . . a second wiring connected to at least one of a source and a drain . . . a second layer including at least one of silicon nitride and nitride oxide silicon formed on and in direct contact with the second wiring, wherein the second wiring formed by fusing conductive nanoparticles.”

Independent claim **11** recites another combination that includes, for example,

“ . . . forming a gate electrode over a substrate having an insulating surface with a droplet discharge method . . . ”

And finally, independent claim **12** recites a further combination that includes, for instance,

“ . . . forming a gate electrode and a connection wiring over a substrate having an insulating surface with a droplet discharge method . . . ”

At the very least, Yudasaka in view of Bojkov, whether taken alone or in combination, fail to disclose or suggest any of these exemplary features recited in independent claims 1-4 and 11-12.

For example, as for claims 1-4, on page 3 of the outstanding Office Action, the Examiner readily admits that Yudasaka fails to disclose a gate electrode formed by fusing conductive nanoparticles. The Examiner turns to the teachings of Bojkov to cure the deficiencies of Yudasaka. In so doing, the Examiner alleges that Bojkov describes a gate electrode formed over a substrate by fusing conductive nanoparticles. However, upon closer

review of Bojkov, the reference merely describes that diamond particles are electrophoretically deposited onto metal lines 1102 (cathode strips). As outlined in column 5, lines 41-50 and FIG. 18 of Bojkov, a continuous diamond layer 1801 is formed by the process of diamond nucleation which occurs primarily onto the diamond particles. Since Bojkov describes that the result of the process effectively reduces, or eliminates cross-talk between metal lines 1102, it should be regarded that diamond is not conductive and, in fact, teaches away from the invention as claimed. Thus, Bojkov does not disclose or fairly suggest that the gate electrode is formed over the substrate by fusing conductive nanoparticles as recited in claims 1-4.

In regard to claims 11 and 12, on page 5 of the outstanding Office Action, the Examiner asserts that Yudasaka describes forming a gate electrode over a substrate having an insulating surface with a droplet discharge method. However, upon review of Yudasaka, the reference fails to disclose or fairly suggest the aforementioned limitation as claimed by the present invention. Yudasaka merely discloses an insulating film forming a TFT, a silicon film and a conductive film formed by applying a solution and annealing it. In a spin coater 102, a coating solution containing a thin film component is spin-coated onto a substrate. The substrate after coating is annealed in an annealing section 103 to form a coating film on the substrate. Yudasaka further discloses that application of the coating solution or a resist by an ink jet process increases utilization of the solution and permits forming a patterned coating film. However, Yudasaka does not disclose forming a gate electrode over a substrate having an insulating surface with a droplet discharge method as recited in claims 11-12. Bojkov is also silent with regard to disclosing this feature as claimed and, therefore, cannot cure the deficiencies of Yudasaka.

The Examiner has failed to establish a *prima facie* case of obviousness for at least four reasons. First, the Examiner has not demonstrated how Yudasaka in view of Bojkov, whether taken alone or in combination, disclose or suggest each and every feature recited in the claims. *See* M.P.E.P. § 2143 (8th ed. 2007). Second, the Examiner has not shown the existence of any reasonable probability of success in modifying Yudasaka, the base reference, based on the teachings of Bojkov, the secondary reference, in a manner that could somehow result in the claimed invention. *See id.* Third, the Examiner has not identified any suggestion or motivation, either in the teachings of the applied references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Yudasaka in a manner that could somehow result in the claimed invention. *See id.* Finally, the Examiner has not explained how his obviousness rationale could be found in the prior art — rather than being a hindsight reconstruction of Applicants' own disclosure. *See id.*

Each of the Examiner's factual conclusions must be supported by “substantial evidence” in the documentary record, as required by the Federal Circuit. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1435 (Fed. Cir. 2002). The Examiner has the burden of documenting all findings of fact necessary to support a conclusion of anticipation or obviousness “less the ‘haze of so-called expertise’ acquire insulation from accountability.” *Id.* To satisfy this burden, the Examiner must specifically identify where support is found within the prior art to meet the requirements of 35 U.S.C. §§ 102(b) and 103. In this case, however, the Examiner has failed to satisfy his burden of demonstrating how Yudasaka, taken alone or in combination with Bojkov, can either anticipate or render obvious each and every one of the limitations present in independent claims 1-4 and 11-12, as required by the M.P.E.P. and Federal Circuit jurisprudence.

In accordance with the M.P.E.P. § 2143.03, to establish a *prima facie* case of obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 409 F.2d 981, 180 USPQ 580 (CCPA 1974). “All words in a claim must be considered in judging the patentability of that claim against the prior art.” In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 196 (CCPA 1970). Therefore, it is respectfully submitted that neither Yudasaka nor Bojkov, taken alone or in any proper combination, discloses or suggests the subject matter as recited in claims 1-4 and 11-12. Hence, withdrawal of the rejection is respectfully requested.

Each of the dependent claims depend from one of independent claims 1-4 or 11-12 and are patentable over the cited prior art for at least the same reasons as set forth above with respect to claims 1-4 and 11-12.

In addition, each of the dependent claims also recites combinations that are separately patentable.

In view of the foregoing remarks, this claimed invention, as amended, is not rendered obvious in view of the prior art references cited against this application. Applicant therefore requests the entry of this response, the Examiner’s reconsideration and reexamination of the application, and the timely allowance of the pending claims.

In discussing the specification, claims, and drawings in this response, it is to be understood that Applicant in no way intends to limit the scope of the claims to any exemplary embodiments described in the specification and/or shown in the drawings. Rather, Applicant is entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation, and applicable case law.

Should the Examiner believe that a telephone conference would expedite issuance of the application, the Examiner is respectfully invited to telephone the undersigned patent agent at (202) 585-8316.

Respectfully submitted,

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